

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-029684

(43)Date of publication of application : 28.01.2000

(51)Int.Cl.

G06F 9/30

G06F 9/355

G06F 9/38

(21)Application number : 11-114756

(71)Applicant : INTERNATL BUSINESS MACH
CORP <IBM>

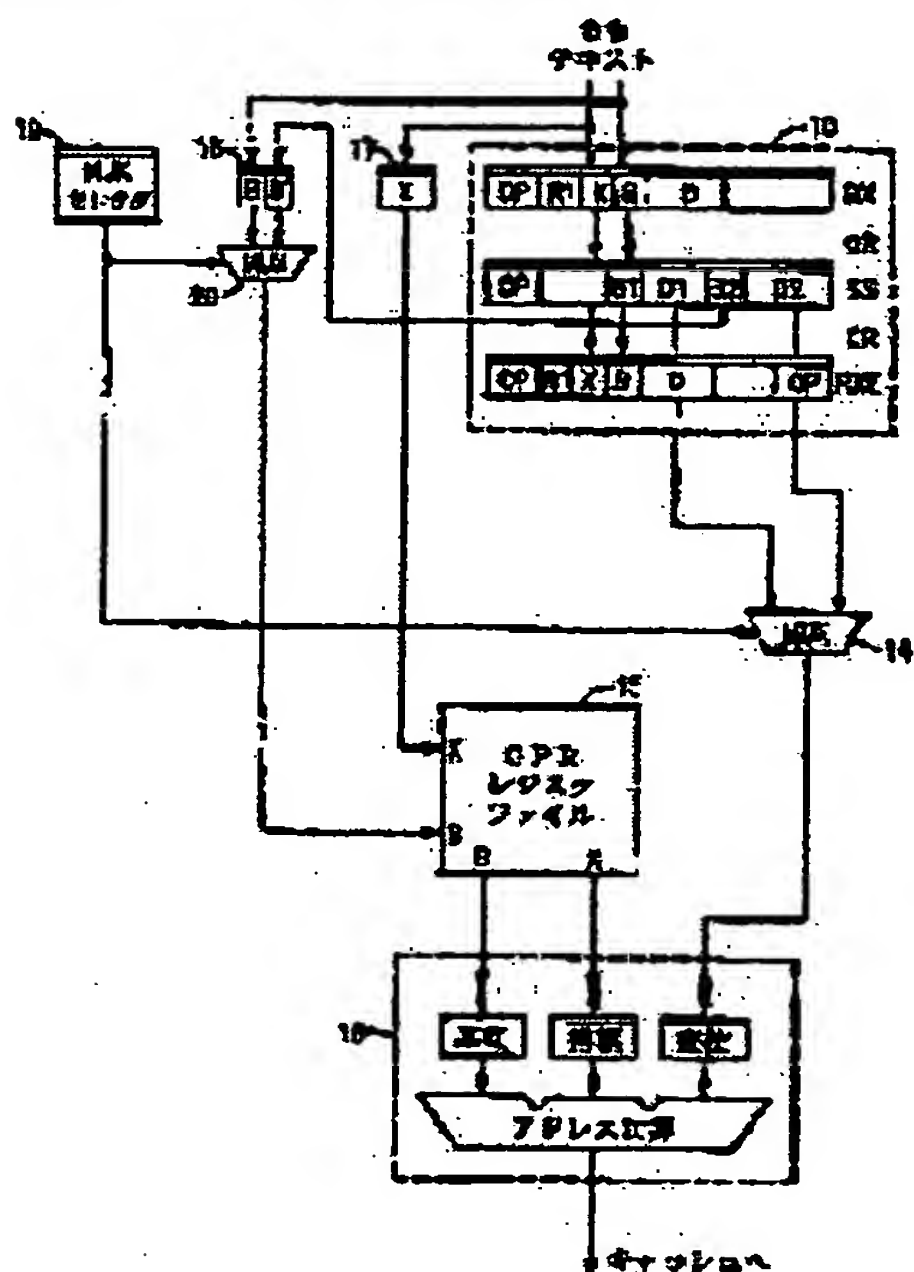
(22)Date of filing : 22.04.1999

(72)Inventor : MARK A CHECK
RONALD M SMITH
JOHN S RIPTY
ERIK M SCHWARZ
TIMOTHY J SLEEGAL
CHARLES F WEBB

(30)Priority

Priority number : 98 70359 Priority date : 30.04.1998 Priority country : US

(54) COMPUTER SYSTEM



(57)Abstract:

PROBLEM TO BE SOLVED: To support a high-frequency operation by arranging the extension of an operation code outside the starting four bytes of an instruction format and assigning a code so that a machine can determine the accurate format of an instruction with only starting light bits of the code.

SOLUTION: As for a base register 18, a multiplexer selector 19 directly controls a base multiplexer 20 and selects and sends a default base position to a CPR register file 15. A 2nd base register is gated from an instruction text to a B prime slot in the base register 18 in a 1st cycle and the multiplexer selector 19 is set to 1. A critical path, therefore, reaches a register for an address adder 16 from the base register 18 through the multiplexer 20 controlled by the selector 19 and the GPR register file 15. Thus, combination logic is excluded from the critical path.